

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Akio MATSUDA, et al.

Application No.:

Group Art Unit:

Filed: September 28, 2001

Examiner:

For: METHOD OF SIMULATING OPERATION OF LOGICAL UNIT, AND COMPUTER-READABLE RECORDING MEDIUM RETAINING PROGRAM FOR SIMULATING OPERATION OF LOGICAL UNIT

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure provisions of 37 CFR § 1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the subject application.

1. Enclosures accompanying this Information Disclosure Statement are:

- 1a. ☒ Form PTO-1449.
- 1b. ☒ Copies of IDS citations.
- 1c. ☐ An English language copy of search report(s) from a counterpart foreign application or a PCT International Search Report.
- 1d. ☐ English language translation (complete or relevant portion(s)) attached to each non-English language publication.
- 1e. ☐ Explanations of Relevancy of References (ATTACHMENT 1(e), hereto) for providing a concise explanation of each non-English publication.

2. ☐ In accordance with 37 CFR § 1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is

(Check appropriate Items 2a, 2b, 2c and/or 2d)

- 2a. ☐ satisfied because all non-English language publications were cited on the enclosed "English-language version of the search report or action which indicates the degree of relevance found by the foreign office". (See MPEP 609, Minimum Requirements for an Information Disclosure Statement, Part A(3): Concise Explanation of Relevance, pp. 600-100 to 600-101, Rev. 1, Feb. 2000.)
- 2b. ☐ set forth in the application.



- 2c. ☐ satisfied because an English language translation (complete or relevant portion(s)) is attached to each non-English language publication.
- 2d. ☐ enclosed as Attachment 1(e), hereto.
3. No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than search report(s) from a counterpart foreign application or a PCT International Search Report, if submitted herewith). 37 CFR §§ 1.97(g) and (h).

Respectfully submitted,

STAAS & HALSEY LLP

Dated: September 28, 2001
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By: 

James D. Halsey, Jr.
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FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.

1075.1174

APPLICATION NO.

FIRST NAMED INVENTOR

Akio MATSUDA, et al.

FILING DATE

September 28, 2001

GROUP ART UNIT

LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

Jc997 U.S. PTO
09/964591

09/28/01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA						
	AB						
	AC						
	AD						
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FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION	
							YES	NO
	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							

OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

AM	K. V. Rompaey, et al., "COWARE – A DESIGN ENVIRONMENT FOR HETEROGENEOUS HARDWARE/SOFTWARE SYSTEMS", (Proceedings EuroDAC), 1996
AN	S. Vernalde et al., "An Object Oriented Programming Approach for Hardware Design ", (IEEE Computer Society Workshop on VLSI) 4/1999.
AO	R. Cmar, et al., "A Methodology and Design Environment For DSP Asic Fixed Point Refinement", (Proceedings Design and Test in Europe Conference, pp. 271-276), 3/1999.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

AM	P. Schaumont, et al., "Hardware Reuse at the Behavioral Level", (The Proceedings of the 36 th Design Automation Conference, ACM, 1999, pp. 784-789) June 1999.
AN	S. Liao, et al., "An Efficient Implementation of Reactivity for Modeling Hardware in the Scenic Design Environment" Proceedings of the Design Automation Conference DAC' 97, pp. 70-75, June 1999.
AO	A. Gerstlauer, et al., "SpecC SYSTEM – Level Design Methodology Applied to the Design of A GSM Vocoder", pp. 19-26, Proceedings of the Workshop on Synthesis and System Integration of Mixed Technologies) April 1999.

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	AM	D. Verkest et al., "On the use of C++ For System on Chip Design" (Proceedings of the IEEE Workshop on VLSI (IWV), pp. 42-47, April 1999.
	AN	A. Fukuda, "Parallel Operating System", pp. 30-32, Issued by Corona Publishing Co., Ltd., 1997
	AO	S. Oaks, et al., "Java Thread Programming, pp. 1-6, Issued by Ohmsha, Ltd., 1997.

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